Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) An apparatus comprising:

a cache of trace information associated with a plurality of traces, each of the plurality of traces including information indicative of interdependent instructions, which interdependent instructions include at least an associated instruction and a criterion instruction that is part of a program sequence and which is data dependent on said associated instruction; and

~~a~~ one or more processors that speculatively execute interdependent instructions associated with a first trace of the plurality of traces as a result of detecting a first triggering condition corresponding to the first trace~~associates first information from the associated instruction with said criterion instruction to form said trace information~~.

2. (Previously Presented) The apparatus of claim 1 wherein the trace information comprises a directed acyclic graph.

3. (Previously Presented) The apparatus of claim 1 wherein the trace information includes pointers to the interdependent instructions.

4. (Cancelled)

5. (Original) The apparatus of claim 1 wherein the interdependent instructions include the criterion instruction and instructions preceding the criterion instruction in the program sequence.

6. (Previously Presented) The apparatus of claim 1 wherein the interdependent instructions are classified into subslice types, the trace information including a pointer to each subslice that is formed by each type of the interdependent instructions.

7. (Original) The apparatus of claim 6 wherein each subslice is stored as dependent pieces.

8. (Currently Amended) The apparatus of claim 1 wherein the ~~information includes a~~ first triggering condition comprises a triggering instruction in the program sequence~~of the trace~~

~~information, the interdependent instructions of the trace being executed when the triggering condition is met~~.

9. (Currently Amended) The apparatus of claim 8 wherein ~~the triggering condition includes a triggering instruction in the program sequence,~~ the first triggering condition ~~being~~ is based on evaluation of an architectural state.

10. (Currently Amended) The apparatus of claim 8 wherein ~~the triggering condition includes a triggering instruction in the program sequence,~~ the first triggering condition ~~being~~ is based on evaluation of a micro-architectural state.

11. (Currently amended) The apparatus of claim 1 ~~wherein the information further includes~~ wherein the one or more processors further determine a confidence metric of ~~the~~ trace information associated with a specific trace, and wherein the confidence metric is indicative of ~~that predicts the~~ a likelihood of producing a correct result from executing the specific trace.

12. (Currently Amended) The apparatus of claim 11 wherein the confidence metric ~~of the trace information~~ indicates whether

or not the specific trace should be replaced by a new trace storing information about different instructions.

13. (Currently Amended) The apparatus of claim 11 wherein the confidence metric ~~of the trace information~~ indicates whether or not the specific trace should be rebuilt using new information about ~~the~~ a criterion instruction associated with the specific trace~~that arrives at the trace cache~~.

14. (Currently Amended) The apparatus of claim 11 further comprising a counter having a counter value that indicates the number of times the specific trace has been executed, the counter value, when exceeding a frequency threshold ~~of~~ associated with the specific trace, triggering the specific trace to be rebuilt.

15. (Currently Amended) The apparatus of claim 1 wherein the plurality of traces includes a second trace and a third trace, wherein the second and third traces ~~that~~ are independent of each other and adjacent in the program sequence, and further comprising ~~are grouped~~ grouping the second trace and the third trace into a very-long-instruction-word ~~for parallel executions~~.

16. (Currently Amended) The apparatus of claim 1 wherein traces of the plurality of traces that are data dependent of each other are chained together for serial executions.

17. (Previously Presented) The apparatus of claim 1 further comprising an instruction pointer that indexes the trace information, the instruction pointer pointing to a first instruction or a last instruction of the interdependent instructions.

18. (Currently Amended) The apparatus of claim 1 further comprising:

a main pipeline executing the program sequence; and at least one secondary pipeline disjoint from the main pipeline configured to speculatively execute ~~executing~~ the interdependent instructions associated with the first trace.

19. (Currently Amended) The apparatus of claim 1 wherein the interdependent instructions associated with the first trace are executed by a secondary thread on a pipeline, and the program sequence is executed by a main thread on the same pipeline.

20. (Currently Amended) A method comprising:

identifying a criterion instruction capable of incurring a potential latency in a program sequence, the potential latency associated with at least one of fetching an instruction associated with an incorrectly chosen branch of the criterion instruction and executing the criterion instruction and incurring a cache miss;

~~capturing the criterion instruction and~~ identifying a pre-selected number of initial candidate instructions preceding the criterion instruction in the program sequence~~,~~;

determining which of the ~~preceding~~ initial candidate instructions ~~and the~~ are associated instructions, wherein an outcome of the criterion instruction depends on the results of the associated instructions~~being interdependent~~; and

storing ~~additional instructions~~ information indicative of the associated instructions and the criterion instruction as trace information in a trace cache ~~relating to said criterion instruction; and~~

~~storing a trace in a trace cache, the trace including information about the criterion instruction interpreted according to said additional instructions and the preceding instructions~~.

21. (Currently Amended) The method of claim 20 wherein the trace information is in a form of a directed acyclic graph.

22. (Currently Amended) The method of claim 20 ~~wherein~~ further comprising determining at least one of whether ~~the~~ a length of the potential latency, ~~includes a long latency that~~ exceeds a predetermined time threshold, ~~a frequent latency that exceeds~~ whether a frequency of the potential latency exceeds a predetermined recurrence threshold, ~~or~~ and whether a variance of the potential latency exceeds a ~~long and uncertain latency that exceeds a mean threshold and a~~ variance threshold.

23. (Currently Amended) The method of claim 20 further comprising dynamically identifying the criterion instruction based on information derived from at least one previous execution~~s~~ of the program sequence.

24. (Currently Amended) The method of claim 20 further comprising capturing the criterion instruction and the ~~preceding~~ associated instructions by copying the criterion instruction and the associated instructions in a buffer.

25. (Currently Amended) The method of claim 20 further comprising locating ~~an~~ existing trace information in the trace cache before storing the trace information, the existing trace information and the trace information to be stored having at least one of the same first instruction or the same last instruction.

26. (Currently Amended) The method of claim 20 further comprising rebuilding the trace information after a duration of time interval that grows each time the trace information is rebuilt until the duration reaches a predetermined time limit.

27. (Currently Amended) The method of claim 20 further comprising storing, in an array, the information indicative of the associated instructions and the criterion instruction as trace information ~~about the criterion instruction and the preceding instructions~~.

28. (Currently Amended) The method of claim 27 wherein the array further includes a subslice type for each of the corresponding criterion instruction and associated instructions, the subslice type being a result of classifying the criterion instruction and associated instructions.

29. (Currently Amended) A computer program residing on a computer readable medium comprising instructions for causing ~~a computer~~ one or machines to to:

identify a criterion instruction incurring a potential latency in a program sequence, the potential latency associated with at least one of fetching an instruction associated with an incorrectly chosen branch of the criterion instruction and executing the criterion instruction and incurring a cache miss;

~~capture the criterion instruction and~~ identify a pre-selected number of initial candidate instructions preceding the criterion instruction in the program sequence~~,~~;

determine which of the ~~preceding~~ initial candidate instructions are associated instructions, wherein an outcome of ~~and~~ the criterion instruction ~~being interdependent~~depends on the results of the associated instructions; and

~~storing~~ storeinformation indicative of the associated instructions and the criterion instruction as trace information in a trace cache. ~~additional instructions relating to said criterion instruction; and~~

~~store a trace in a trace file, the trace including information about the criterion instruction interpreted according to said additional instructions, the preceding~~

~~instructions, and interdependency among the criterion instruction and the preceding instructions.~~

30. (Original) The computer program of claim 29 wherein an analysis window defined in the computer program causes the computer to capture the criterion instruction and ~~preceding~~ initial candidate instructions.

31. (Original) The computer program of claim 29 wherein the computer identifies the criterion instruction by profiling the program sequence.

32. (Currently Amended) The apparatus as in claim 1, wherein there are multiple associated instructions associated with ~~said~~ a criterion instruction of the first trace, and said processor forms first trace information using a first of said associated instructions, and second trace information using a second of said associated instructions.

33. (Currently Amended) The apparatus as in claim 1, wherein said criterion instructions are capable of incurring a potential latency in the program sequence, the~~instructions which represent relatively long latencies in execution~~potential

latency associated with at least one of fetching an instruction associated with an incorrectly chosen branch of the criterion instruction and executing the criterion instruction and incurring a cache miss.

34. (Previously Presented) The apparatus as in claim 1, wherein the criterion instructions include template data for an instruction form, and the associated instructions include information that assigns values of register information within the criterion instructions.

35. (Currently Amended) The method as in claim 20, further comprising associating multiple different associated instructions with said criterion instruction, and wherein said storing ~~comprising forms~~ comprises storing first trace information ~~using~~ indicative of a first of said associated instructions, and second trace information ~~using~~ indicative of a second of said associated instructions.

36. (Currently Amended) The method as in claim 20, wherein said ~~execution~~potential latency includes a time to unload the instruction associated with the incorrectly chosen branch of the criterion instruction from a pipeline.~~criterion instructions are~~

~~instructions which represent relatively long latencies in execution~~.

37. (Previously Presented) The method as in claim 20, wherein the criterion instructions include data for an instruction form, and said storing comprising associating information from said additional instructions as register information within the criterion instructions.

38. (Currently Amended) A program as in claim 29, further comprising associating multiple different associated instructions with said criterion instruction, and wherein said instructions cause the one or machines to ~~said storing comprising forms~~ store first trace information using a first of said associated instructions, and further to store second trace information using a second of said associated instructions.

39. (Currently Amended) A program as in claim 29, wherein said ~~criterion instructions are instructions which represent relatively long latencies in execution execution~~potential latency includes a time to unload the instruction associated with the incorrectly chosen branch of the criterion instruction from a pipeline.

40. (Cancelled)